SUBCONTRACT TITLE: ***ADVANCED PROCESSING OF CdTe- AND $CuIn_XGa_{1-X}Se_2$-BASED SOLAR CELLS***

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REPORT FOR: Phase II/Quarter I

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This is the progress report for the 1st quarter of Phase II for the months of January '03 through March '03. The project covers two thin film technologies: CdTe and CIGS. The focus areas include: (a) CdTe – stability, novel back/front contacts, and the development of manufacturing friendly processes; (b) CIGS – development of two-step non-co-evaporation technology.

A. CdTe

Stability

Effect of $CdCl_2$ Heat Treatment

Most of the results from light soaking experiments for cells $CdCl_2$ heat treated at different temperatures were included in a previous report. We collected additional data that supplement/update the previous observations and are presented here with a summary of what was reported previously. The summarized observations for the samples $CdCl_2$ heat treated at different temperatures and light soaked for 1000 hours are:

- Samples annealed at the lowest temperature (360°C; lowest initial performance) exhibited the largest increase in their dark currents. The dark current increase was due to both (dark) "shunting" and an increase in the recombination current.
- Samples annealed at or close to optimum (390°C) temperatures exhibited no (or very small) increase in their dark current. In some cases no shunting or increased recombination was observed. The smallest overall changes in the dark current (and solar cell characteristics) were associated with devices processed at 390°C.
- In general, changes in samples held at OC were larger in magnitude than for cells held at SC, although the type of changes was the same (i.e. increase in the dark current).
- All cells exhibited an increase in their series resistances (both dark and light) which was gradual and consistent over the duration of the experiment, suggesting a possible increase in the bulk resistivity of the semiconductors.
- The timing of the observed changes varied, however, after 1000 hours nearly all observed changes, in particular increases in the dark current, were consistent and similar in magnitude for the specific samples/conditions.

It was also mentioned that the observed dark shunting was not detrimental to solar cell performance since under light the shunt resistances did not appear to decrease significantly.

However, after measuring all devices it appears that the cells heat treated at the lowest temperature(s) (and which exhibited the largest increase in their dark current) did show a decrease in their light shunt resistance, enough to have a significant effect on the FF. Table 1 below lists the measured series and shunt resistances for the above discussed samples (light soaked @ OC). It should be noted that the data in this table are averages for all light soaked devices (excluding those that catastrophically failed). As indicated above the series resistance increased, and the shunt resistance decreased significantly for cells heat treated at temperatures lower than the optimum one. The series resistances were estimated from the slope of the J-V at high currents and the shunt resistance from the slope at a reverse bias voltage of 1.5-2.0 volts.

Table 1. Initial and final (1000 hrs of light soaking @ OC) light series and shunt resistances.

Annealing T [°C]	Initial $R_{S\ LIGHT}$ [Ω-cm^2]	Final $R_{S\ LIGHT}$ [Ω-cm^2]	Initial $R_{SH\ LIGHT}$ [Ω-cm^2]	Final $R_{SH\ LIGHT}$ [Ω-cm^2]
360	3.03	3.40	2500	460
380	2.53	3.0	2300	590
390	3.0	2.5	3500	6100
400	1.90	3.40	2100	1700

Effect of Cu – New Set of Devices

A second set of devices is currently being fabricated in order to begin a new light soaking experiment. The objective this time is to attempt to quantify the impact of Cu. The cells in this case are being fabricated using a contacting approach similar to what other groups have used (are using), where Cu is deposited onto the CdTe surface prior to the deposition of the back electrode (the CdTe surface is etched in a bromine/methanol solution prior to the Cu application). This approach was chosen over the baseline doped graphite process in order to better control the amount and uniformity of copper over the area of the cell. Sputtering is being used for the deposition of Cu the thickness of which is being varied from 5 to 80 Å. The samples are subsequently masked, contacted with graphite paste (undoped) and heat treated. The temperature of the heat treatment is being varied from a low of 150 to a high of 300°C. An

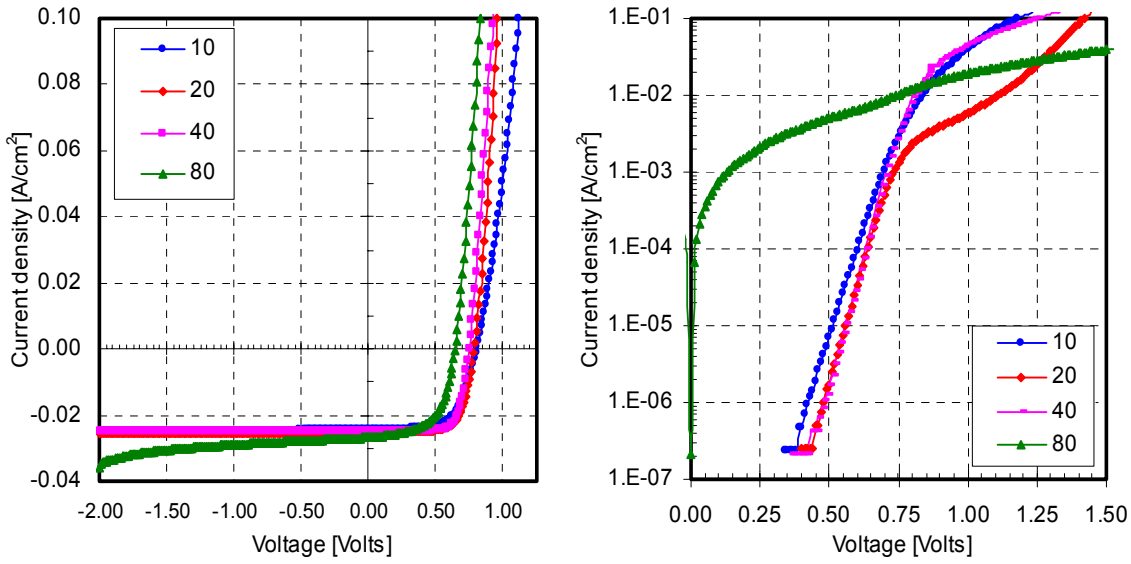

Figure 0. Light and dark J-V characteristics for cells contacted with Cu of different thicknesses and heat treated at 225°C.

example of a series of devices heat treated at 225°C after depositing Cu of different thicknesses is shown in Fig. 1. The Cu thickness for these cells was: 10, 20, 48, and 80 Å (as indicated in the legend). The range of V_{OC} and FF values is listed in table 2. The V_{OC} decreases with increasing Cu thickness. Based on the dark Ln(J)-V these devices, the three smallest Cu thicknesses result in no apparent dark shunting and very similar dark J-V characteristics (instrumentation limitations are currently limiting current measurements to approx. 10^{-7}-10^{-8} A). Nevertheless the variations in FF and V_{OC} for these three are significant. The device with the smallest Cu thickness (10 Å) is slightly limited by a back barrier as indicated by the behavior of its light J-V near V_{OC}, which affects the FF. The device with 40 Å of Cu has the lowest dark current (very similar to the cell with 20 Å) which leads to the highest FF (its V_{OC} is about 20-40 mV lower than the best obtained in this set of devices). The most significant difference among the four cells is in the "dark" and "light" shunting where the device with the largest Cu thickness has the smallest shunt resistance of all (the dark current for this cell is nearly 5 orders of magnitude higher than the others). This group of devices is representative of what is being observed for the all cells fabricated with this contact, with this annealing temperature currently being the "optimum" from a performance point of view. This work continues in order to develop a larger set of samples suitable for the next round of light soaking experiments.

Table 2. The range of V_{OC} and FF values for all devices originating from the substrates represented in Fig. 1.

Cu Thickness [Å]	V_{OC} [mV]	FF
10	800-810	60-64
20	780-810	64-72
40	740-760	70-76
80	640-670	58-65

Vapor Chloride Treatment

A larger area vapor annealing apparatus has been brought on-line. Based on the encouraging results and the simplicity of the vapor treatment process the initial objective is to demonstrate uniformity and reproducibility in solar cell performance, with the ultimate objective to produce a large number of devices in order to study the effect of this treatment on cell stability. Initial devices processed in the new annealing chamber have yielded devices with lower performance than what was obtained in the small area apparatus using the same conditions. Currently the emphasis is on understanding what limits the performance of these devices and re-optimizing the vapor treatment process for the large area apparatus.

In the meantime the small apparatus is also being utilized with the latest experiments dealing with the effect of the temperature of the $CdCl_2$ source, which essentially determines the partial pressure of the $CdCl_2$ during the treatment. The effect of the substrate temperature has been described in previous reports. Figure 2 shows the V_{OC} of vapor-treated devices where the source annealing temperature was varied as indicated in the figure. The FF for the same cells did not exhibit similar trends and this is believed to be related to the condition of the CdTe surface[†]. The cells on the right exhibited improved performance suggesting that increasing the $CdCl_2$ partial pressure is beneficial. Based on the fact that longer annealing times lead to lower performance, it was expected that increasing the $CdCl_2$ vapor pressure would also have a similar effect due to "over-exposure" of the samples. The effect of the $CdCl_2$ vapor pressure is not fully understood at this time and it will be the subject of future work.

[†] The cells shown in Fig. 2 were not etched prior to the formation of the back contact.

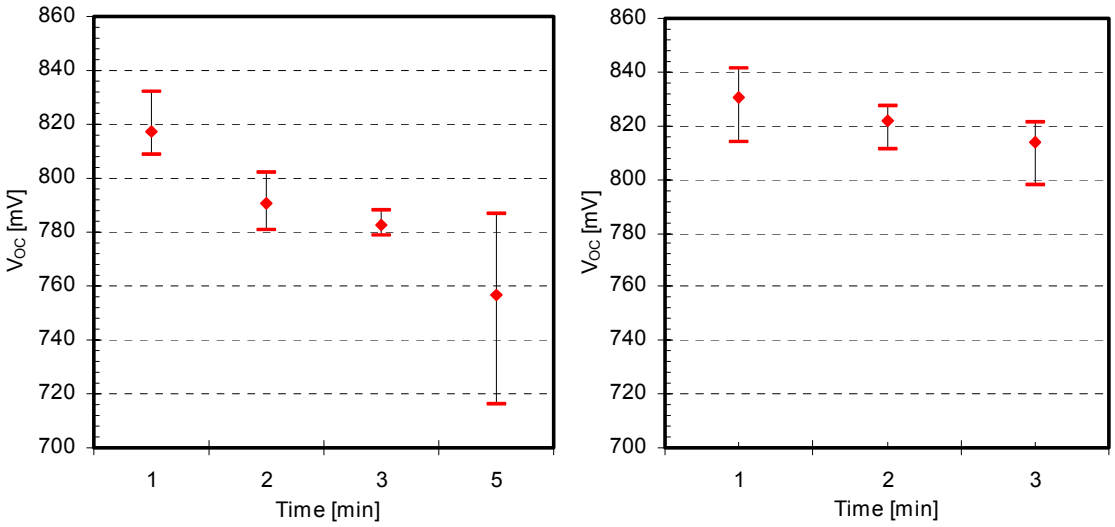

Figure 0. The V_{OC} of cells treated with $CdCl_2$ vapors using different source ($CdCl_2$) temperatures: Left – 460°C; right – 500°C.

TCO's/Buffer Layers

Work in this area continues with recent emphasis being placed on In_2O_3 and Zn_2SnO_4 buffer layers. Indium oxide was found to be a promising buffer as previously reported and more recent work has been focusing on the effect of the CdS thickness in devices where In_2O_3 is used as a buffer. In the case of Zn_2SnO_4 films, although some encouraging initial results have been obtained, more work is needed in order to optimize these films and better control their composition. Figure 3 shows SR measurements on Zn_2SnO_4 based devices. These cells are from a batch processed to evaluate the effect of heat treating the TCO bi-layer structure. Despite the thin CdS (based on the blue response) the V_{OC} for these devices exceeded the 820 mV mark. Additional cell results will be presented in future reports.

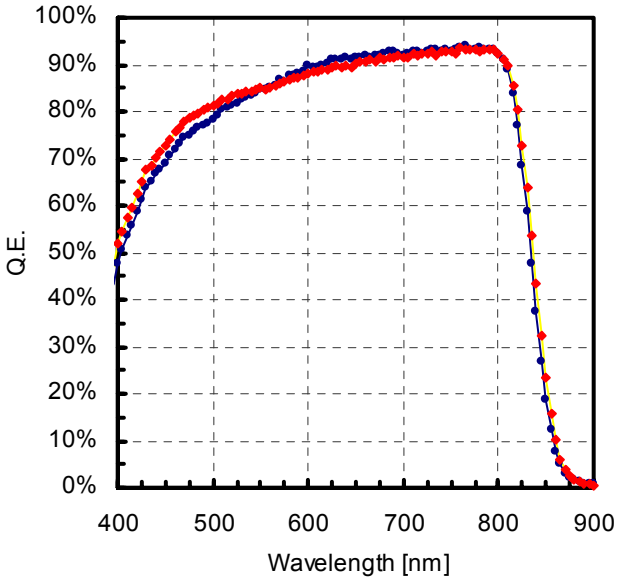

Figure 0. Spectral response of CdTe solar cells with Zn_2SnO_4 as a buffer

Large Area Deposition System

Devices are now routinely being fabricated using the large area deposition system. Initial depositions were being carried out on moving substrates (i.e. the substrate is continuously moving over and past the source during the deposition process). However, in order to address uniformity issues, currently the substrates are moved over the source to initiate the deposition process once the desired temperatures are reached, kept stationary over the source for 1-2

minutes, and moved past the source in order to end the deposition process. This approach has helped improved the uniformity of the films. The V_{OC} uniformity (for partially optimized conditions) also improved and deposition runs are now yielding cells with V_{OC}'s over 810 mV; (typical variations are within 10 mV; 820-830 mV). However, the FF needs to be further improved. Although it has reached values of 72%, it is typically in the high 60's, with large frequent variations on the order of 5%. One reason for these variations is shunting which appears to vary significantly from cell to cell; the shunting is "enough" to significantly affect the FF but not V_{OC}. The cause of this is either the CdTe film itself (density variations) or variations in the composition of the back contact[†]. This issue is currently being addressed.

Material utilization for the large area deposition process has been found to be in the 30-50% range. Although it would be desirable to further improve on this parameter this may not be possible with the current source-substrate design.

[†] Recent imaging of USF cells done at UT revealed "hot" spots which may be related to non-uniformities in the composition of the graphite paste.

B. CIGS

One of the challenges that we continue to face with our 2-step processing approach is controlling defects. As discussed on several occasions, a particular issue is the effective incorporation of Ga. We can get Ga into the space charge layer, and we can get it to bond to open the band gap. However, in doing so we seem to always increase the defect level. While we have made progress in reducing defect levels, we still have not reduced them sufficiently to achieve the level of desired performance. If we knew what the controlling defects are, this may lead to process modifications that could control them. Unfortunately, there is no direct way to determine exactly what the defects are at such low levels. Instead we must use indirect techniques that rely upon various types of input. We can measure the effect of defects on electronic properties with techniques such as photocapacitance[1]. This also helps us understand the relationship between the defects that we sense and film composition as well as the relationship between composition and device performance. These insights have lead to improvements in processing and in performance, but more needs to be done.

To aid our experimental efforts we rely as well upon guidance provided by simulation. In our earlier efforts much of our device modeling was based upon assumed dominance by deep levels[2]. This resulted in good agreement with experimental results and to some extent helped point the way to new wrinkles in processing. However, as we all know, models that fit a set of data are rarely unique, and in this case we did not know what the deep level was that we were using as the basis for modeling. Materials modeling by the NREL Theory Group is assisting these efforts by providing insights to likely defects in CIGS[3]. In Quarterly Report 5 of year 3 in the predecessor to this project we presented modeling results based upon use of the primary defect levels identified by the NREL Theory Group[3]. The defects with the lowest formation energies are the V_{Cu} and the M_{Cu} + $2V_{Cu}$ defect pair. The V_{Cu} is acceptor-like, and the defect pair is donor-like. Both are shallow, and thus compensation effects are operative. (A full discussion of this can be found in the earlier report). What we want to pick up on here is the result that indicated a difference in dark IV curves when one or the other of these defects is dominant. In figure 1 we show an extended version of that result. The lines are simulations for varying levels of compensation. The lowest lying line is the ideal case of no defects. The device band gap is 0.95 eV, so with an expected Jsc of 40 mA/cm^2 extrapolation of the dark IV would result in an expected Voc of 600 mV. The solid line is the dark IV that results from fitting the power curve of one of our top-end devices. To fit the data for these devices requires about 40% compensation. The top-most line is for full compensation, and the one below it is for 80% compensation. As can be seen, as the level of compensation increases, the dark IV shifts upward and thus lowers Voc. However, at the highest compensation levels there is

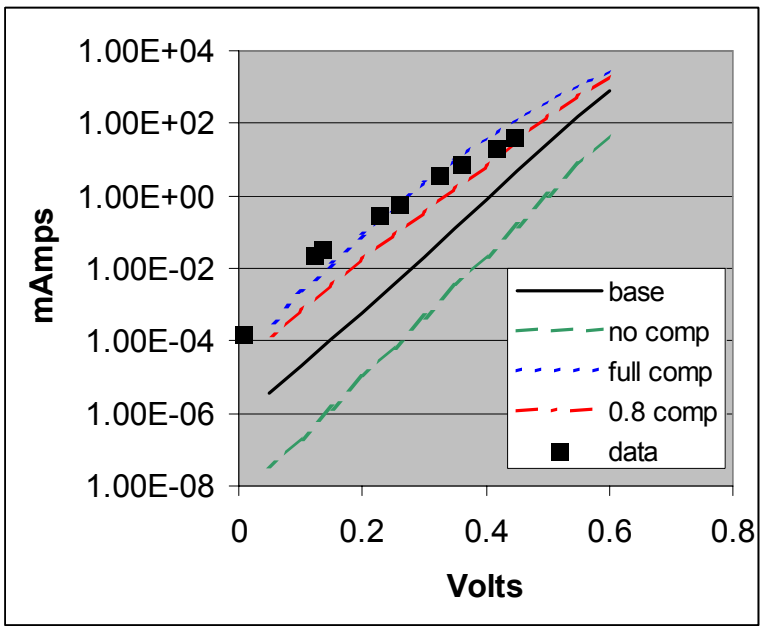

Figure 0. Simulated and experimental IV curves for devices with various levels of compensation.

bending over at high voltages which reduces the expected loss. Based upon these observations we feel that the dark IV may be a telltale that indicates the level of compensation, and thus indirectly suggests the operative defects.

Since the results in figure 1 only involve shallow levels, there is a suggestion that deep levels may not be operative as originally thought. To sort this out we are starting to look more carefully at dark IV data. The data points(□) in figure 1 are experimental data from a device with Voc of about 425 mV. The data is from Isc –Voc plots. This eliminates contributions from series resistance allowing a more direct look at junction properties. As can be seen, the data falls near the curve for complete depletion, but seems to bend over a bit more at high voltage. If the behavior is explainable only by the shallow states used for the simulations in figure 1, then it would be between 80% and 100% compensated. In figure 2 we show the simulation of the junction region for 40% and 80% compensation. As can be seen, the space charge width increases from about 200 nm to 450 nm over this range of compensation. At full compensation, the device would be completely depleted which would result in more unusual behavior. However, 80% compensation with a space charge width of 400 – 500 nm is not unrealistic. 200 – 500 nm is typically what we observe. This model would result in a direct correlation between Voc and capacitance. That is, as compensation increases, the space charge width increases resulting in decreasing capacitance and correspondingly decreasing Voc. We have observed such behavior previously in our photocapacitance studies[1], but based on the then current model were attributing it to deep states. These new observations suggest that shallow states may be playing a role as well because of their compensation effects.

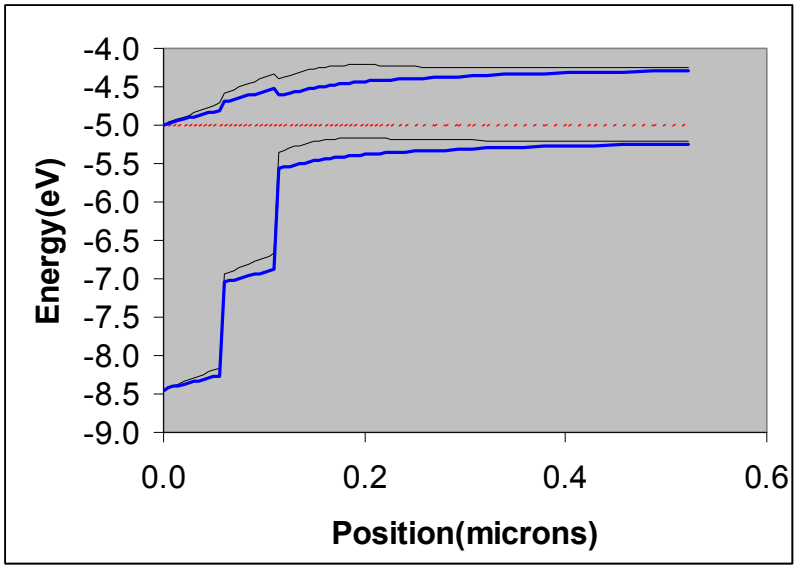

Figure 0. Simulation of junction region in CIGS for 40%(light line) and 80% (heavy line) compensation.

It now becomes important to distinguish between contributions from deep and shallow states if we are to fully understand what is going on. The near fit of the data to the shallow state simulations is suggestive, but just a start. The bend over in the data seems to favor additional mechanisms. In particular, deep states can produce such behavior[2]. A comparison of diode factor behavior for deep and shallow states is shown in figure 3 from our earlier simulation efforts. As can be seen, shallow levels(at Ec – 0.27 eV) produce low diode factors and thus steep IV curves like those in figure 1. However, mid-gap levels produce diode factors which become large in certain voltage ranges and thus can produce the kind of bend over (small slopes) seen in figure 1. A more direct comparison can be made by observing the experimental diode factor in figure 4. This is from the data in figure 1. The behavior is seen to be much more like the mid-gap simulation in figure 3 than the shallow state simulation and thus favors contributions from deep states.

Although there appears to be support for deep state contributions in the experimental data, determining what these states might be is not straightforward. What one would look for is a defect near mid-gap with low formation energy. There is no obvious answer here based upon the defect properties from the NREL theory group. To sort this out will take a considerable amount of data and analysis and some measure of luck. Before getting that specific, however, we need to first address the relative contributions from deep levels versus compensation from shallow levels. An update will be provided in future reports.

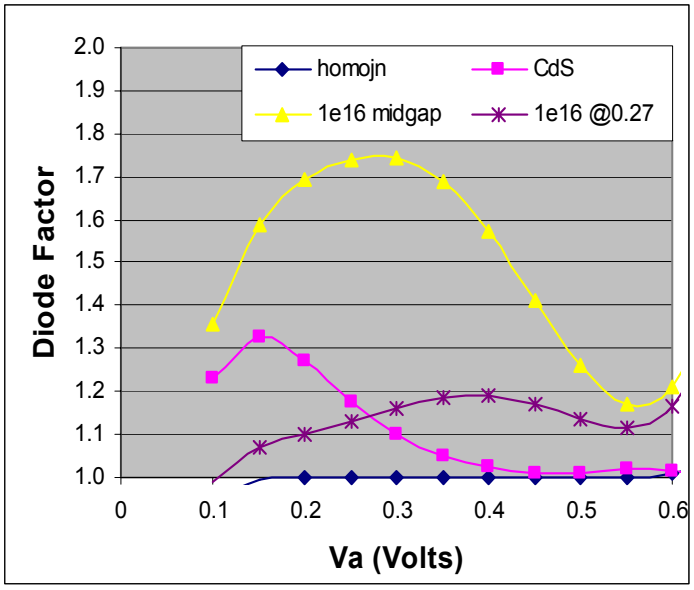

Figure 3. Simulations of diode factor for various junction configurations.

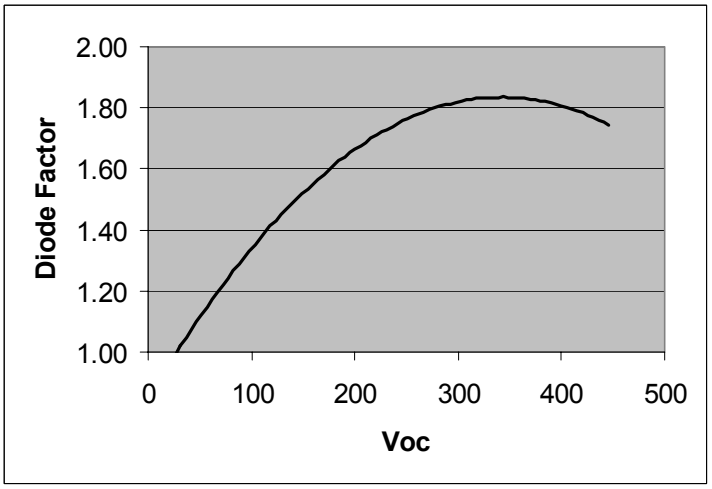

Figure 4. Experimental diode factor voltage dependence.

References

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3. Su-Huai Wei, S. B. Zhang, and Alex Zunger, *Appl. Phys. Lett.*, **72**(4), 3199 (1998).